

<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200208596-1	10/1635283	
	APPLICANT		
	Tyson R. McGuffin		
FILING DATE		GROUP	
		2825	

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
B	1A	5,880,967	03/09/1999	Jyu, et al.	
B	1B	5,949,723	09/07/1999	Clemen, et al.	
B	1C	6,097,207	08/01/2000	Bernstein, et al.	
B	1D	6,209,122 B1	03/27/2001	Jyu, et al.	
B	1E	6,339,835 B1	01/15/2002	Reddy, et al.	
B	1F	6,513,145 B1	01/28/2003	Venkitakrishnan	
B	1G	6,518,796 B1	02/11/2003	Stan, et al.	
	1H				
	1I				
	1J				
	1K				

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

B	1Q	Paul Wiley, et al., "Building Robust, Reliable Nanometer ICs", EEdesign An EE Times Community, July 1998, pp. 1-8.
B	1R	Synopsys Products & Solutions, "PathMill: Transistor-Level Static Timing Analysis", www.synopsys.com/products/analysis/pathmill_ds.html, March 8, 2000, pp. 1-3.
B	1S	Synopsys PathMill--Datasheet, "PathMill DataSheet: Critical Path and Static timing Analysis", idcc.kaist.ac.kr/CAD/epic/pathmill.html, Synopsys, Inc. October 13, 1997, pp. 1-4.

EXAMINER

DATE CONSIDERED

11/21/05

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200310257-1

APPLICATION NO.

10/635283

CONFIRMATION NO.

APPLICANT

Thomas W. Chen

FILING DATE

GROUP

8825

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A			
	1B			
	1C			
	1D			
	1E			
	1F			
	1G			
	1H			
	1I			
	1J			
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	1L				
	1M				
	1N				
	1O				
	1P				

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

1Q	Synopsis Products & Solutions, "AMPS Datasheet Intelligent Design Optimization", www.synopsys.com/products/analysis/amps_ds.html, Synopsys, Inc. November 29, 1999, pp. 1-3
1R	Tanay Karnik, et al., "Total Power Optimization By Simultaneous Dual-Vt Allocation and Device Sizing in High Performance Microprocessors", ACM, June 2002
1S	Michel Crote, Philippe Hurat, "Better Cells for Better Designs Power and Performance Optimization of Cell-Based Designs with Transistor-level Cell Sizing, Chapter 9, pp. 1-16

EXAMINER

DATE CONSIDERED

B. H. Lee

11/27/05